3. The AlGaN/GaN HEMT of claim 1, the buffer layer is disposed on the substrate over a nucleation layer comprised of GaN or AlN.

4. The AlGaN/GaN HEMT of claim 1, the EBB region of implanted fluorine is located in a region of the heterostructure under the prospective location for a gate of the heterostructure.

5. The AlGaN/GaN HEMT of claim 1, the implanted fluorine comprises implanted Fluorine-19 ions delivered to the heterostructure with an energy and at a dose substantially equivalent to 50 kilo electron Volts and 10^{12} ions per square centimeter.

6. The AlGaN/GaN HEMT of claim 1, the implanted fluorine comprises a peak fluorine concentration located in the buffer layer adjacent to the interface.

7. The AlGaN/GaN HEMT of claim 1, the substrate comprises sapphire, the buffer layer comprises unintentionally doped GaN, and the barrier layer comprises one of unintentionally or intentionally doped AlGaN.

8. The AlGaN/GaN HEMT of claim 7, the buffer layer comprises approximately 2 micrometers of unintentionally doped GaN, and the barrier layer comprises approximately 24 nanometers of unintentionally doped AlGaN.

9. The AlGaN/GaN HEMT of claim 1, further comprising:

a low density drain region of fluorine adjacent to the prospective location for the gate of the HEMT and between the prospective location for the gate of the HEMT and the prospective location for the drain of the HEMT.

10. The AlGaN/GaN HEMT of claim 9, the EBB region of implanted fluorine is located in a region under the prospective location for the gate of the HEMT and extends substantially towards a region under the prospective location for the source of the HEMT.

11. An Aluminum Gallium Nitride/Gallium Nitride (AlGaN/GaN) vertical heterostructure field-effect transistor (V-HFET) structure, comprising:

an unintentionally doped gallium nitride (GaN) layer;

an aluminum gallium nitride (AlGaN) layer disposed on the GaN layer and forming a heterojunction at an interface of the AlGaN layer and the GaN layer; and

at least one fluorine implanted blocking region disposed within the GaN layer and extending across a portion of the heterojunction.

12. The AlGaN/GaN V-HFET structure of claim 11, the at least one fluorine implanted blocking region comprises a peak fluorine concentration located in the GaN layer adjacent to the interface.

13. A method of forming a back barrier region in a high electron mobility transistor (HEMT), the HEMT having at least one design location for a source, a gate, and a drain of the HEMT, the method comprising:

depositing a buffer layer over a substrate;

depositing a barrier layer over the buffer layer to form a heterojunction; and

implanting fluorine ions into the buffer layer to form at least one back barrier region under the at least one design location for the gate.

14. The method of claim 13, the implanting includes implanting the fluorine ions to establish a peak fluorine concentration located in the buffer layer adjacent to the heterojunction.

15. The method of claim 13, the depositing of the buffer layer includes epitaxial crystal buffer layer growing of approximately 2 micrometers of unintentionally doped gallium nitride (GaN) and the depositing of the barrier layer includes epitaxial crystal barrier layer growing of approximately 24 nanometers of unintentionally doped aluminum gallium nitride (AlGaN).

16. The method of claim 13, the implanting includes implanting Fluorine-19 ions that have been imparted with an energy and at a dose substantially equivalent to 50 kilo electron Volts and 10^{12} ions per square centimeter.

17. The method of claim 13, the depositing of the buffer layer includes growing the buffer layer over at least one of a sapphire substrate, a silicon (111) substrate, a silicon carbide (SiC) substrate, an aluminum nitride (AlN) substrate, or a Gallium Nitride (GaN) substrate.

18. The method of claim 13, the depositing of the buffer layer includes growing the buffer layer over the substrate having a Gallium Nitride (GaN) nucleation layer or an Aluminum Nitride (AlN) nucleation layer.

19. The method of claim 13, further comprising:

incorporating fluorine ions within the barrier layer to form an enhancement mode HEMT.

20. The method of claim 13, further comprising:

forming a low density drain region of fluorine adjacent to a design location of the gate and between the design location of the gate and a design location of the drain.

21. The method of claim 20, the implanting includes implanting the fluorine ions into the buffer layer to form the back barrier region under the design location of the gate and reaching to a region under a design location of the source.

22. An enhancement mode high electron mobility transistor (HEMT), comprising:

a buffer layer;

a barrier layer disposed over the buffer layer at an interface of the barrier layer and the buffer layer;

at least one fluorine blocking region disposed within the buffer layer and extending across a portion of the heterojunction; and

at least one fluorine treated region in the barrier layer.

23. The enhancement mode HEMT of claim 23, the at least one fluorine blocking region comprises a peak fluorine concentration located in the buffer layer adjacent to the interface.

24. The enhancement mode HEMT of claim 23, the at least one fluorine treated region comprises a low density drain region of fluorine adjacent to a design location of a gate and between the design location of the gate and a design location of a drain of the HEMT.

25. The enhancement mode HEMT of claim 23, the at least one fluorine treated region comprises a region of fluorine disposed within the barrier and below the design location of the gate.

26. The enhancement mode HEMT of claim 23, the at least one fluorine treated region comprises a region of fluorine implanted by at least one of a fluorine plasma treatment or low energy ion implantation.

* * * * *